CLAIMS

1. A method comprising:

calculating a first delay value representing an estimated delay between an input signal and a fed back signal, said first delay value comprising a whole number of sample cycles;

calculating a second delay value from said first delay value, said second delay value comprising a fraction of a sample cycle; and

adding the first delay value and the second delay value to generate a third delay value representing a more precise estimated delay between the input signal and the fed back signal.

2. The method of claim 1, wherein said calculating the first delay value comprises oversampling the input signal.

3. The method of claim 2, wherein the input signal is oversampled at a sampling rate of thirty-two samples per symbol, and wherein the first delay value comprises a whole number between one and thirty-two.

4. The method of claim 2, wherein said calculating the first delay value further comprises solving the equation:

$$D = \arg\max_{d} \left\{ Corr\left(V_m(t-d), V_f(t)\right) \right\}$$

where

$$Corr\left(V_m(t), V_f(t)\right) = C(n) = \frac{1}{N-d} \sum_{n=d+1}^{N-1} V_m(n-d) V_f^*(n)$$

where D is the first delay value, V_m is the input signal, and V_f is the fed back signal.

5. The method of claim 1, wherein said calculating the second delay value comprises solving the equation

$$a = -\frac{\sum_{t=1}^{N} Z^*(t) X(t) + Z(t) X^*(t)}{2\sum_{t=1}^{N} Z(t) Z^*(t)} = -\frac{\sum_{t=1}^{N} \Re\left\{ Z^*(t) X(t) \right\}}{\sum_{t=1}^{N} \left| Z(t) \right|^2}$$

where

$$Z(t) \equiv K\left[V_m(t-D-1) - V_m(t-D) \right]$$

where

$$X(t) \equiv V_f(t) - K V_m(t-D-1)$$

where K is the linear gain factor, D is the V_m is the input signal, and V_f is the fed back signal.

6. The method of claim 1, further comprising decrementing the first delay value by one and recalculating

the second delay value with the decremented first delay value in response to the second delay value being less than one.

7. The method of claim 1, further comprising incrementing the first delay value by one and recalculating the second delay value with the incremented first delay value in response the to the second delay value being greater than one.

8. The method of claim 1, further comprising modulating the input signal for transmission from a Personal Digital Communications (PDC) transmitter.

9. The method of claim 8, further comprising calculating the first delay value in two slots.

10. The method of claim 8, further comprising calculating the second delay value in four slots.

11. An apparatus comprising:

an antenna;

a modulation path having an input operative to receive an input signal, said modulation path operative to modulate said input signal and output a modulated signal for transmission from the antenna;

a feedback path operative to generate a feedback signal from the modulated signal; and

a predistorter connected between the feedback path and the input of the modulation path, said predistorter comprising a delay estimator operative to

calculate a first delay value representing an estimated delay between the input signal and the feedback signal, said first delay value comprising a whole number of sample cycles,

calculate a second delay value from said first delay value, said second delay value comprising a fraction of a sample cycle, and

add the first delay value and the second delay value to generate a third delay value representing a more precise estimated delay between the input signal and the feedback signal.

12. The apparatus of claim 11, further comprising a look-up table connected between the predistorter and the input of the modulation path, said look-up table including a plurality of predistortion values.

13. The apparatus of claim 12, further comprising a PDC transmitter section.

14. The apparatus of claim 12, wherein the look-up table comprises a 256x2 array.

15. The apparatus of claim 12, wherein the predistorter is operative to generate the first delay value within two slots.

16. The apparatus of claim 12, wherein the predistorter is operative to generate the second delay value within four slots.

17. A article comprising a machine-readable medium which stores machine-executable instructions, the instructions causing a machine to:

calculate a first delay value representing an estimated delay between an input signal and a fed back signal, said first delay value comprising a whole number of sample cycles;

calculate a second delay value from said first delay value, said second delay value comprising a fraction of a sample cycle; and

add the first delay value and the second delay value to generate a third delay value representing a more precise estimated delay between the input signal and the fed back signal.

18. The article of claim 17, wherein the instructions causing the machine to calculate the first delay value comprise instructions causing the machine to oversample the input signal.

19. The article of claim 18, wherein the input signal is oversampled at a sampling rate of thirty-two samples per symbol, and wherein the first delay value comprises a whole number between one and thirty-two.

20. The article of claim 18, wherein the instructions causing the machine to calculate the first delay value further comprise instructions causing the machine to solve the equation:

$$D = \arg\max_{d} \left\{ Corr\left(V_m(t-d), V_f(t)\right) \right\}$$

where

$$Corr\left(V_m(t), V_f(t)\right) = C(n) = \frac{1}{N-d} \sum_{n=d+1}^{N-1} V_m(n-d) V_f^*(n)$$

where D is the first delay value, Vm is the input signal, and Vf is the fed back signal.

21. The article of claim 17, wherein the instructions causing the machine to calculate the second delay value

further comprise instructions causing the machine to solve the equation:

$$a = -\frac{\sum_{t=1}^{N} Z^*(t)X(t) + Z(t)X^*(t)}{2\sum_{t=1}^{N} Z(t)Z^*(t)} = -\frac{\sum_{t=1}^{N} \Re\{Z^*(t)X(t)\}}{\sum_{t=1}^{N} |Z(t)|^2}$$

where

$$Z(t) \equiv K\left[V_m(t-D-1) - V_m(t-D)\right]$$

where

$$X(t) \equiv V_f(t) - KV_m(t-D-1)$$

where K is the linear gain factor, D is the Vm is the input signal, and Vf is the fed back signal.

22. The article of claim 17, further comprising instructions causing the machine to decrement the first delay value by one and recalculate the second delay value with the decremented first delay value in response to the second delay value being less than one.

23. The article of claim 17, further comprising instructions causing the machine to increment the first delay value by one and recalculate the second delay value with the incremented first delay value in response to the second delay value being greater than one.

24. The article of claim 17, further comprising instructions causing the machine to modulate the input signal for transmission from a Personal Digital Communications (PDC) transmitter.

25. The article of claim 24, further comprising instructions causing the machine to calculate the first delay value in two slots.

26. The article of claim 24, further comprising instructions causing the machine to calculate the second delay value in four slots.

27. A method comprising:

providing a signal path for a first signal at a first input of a multiplier through a Digital-to-Analog Converter (DAC), a modulator and a power amplifier; and

providing a feedback signal path for a second signal from the power amplifier through a demodulator and an Analog-to-Digital Converter (ADC) to a second input of the multiplier.

28. The method of claim 27 further comprising providing a time delay for the second signal in the

feedback signal path that compensates for the time delay of the first signal in the signal path.

29. The method of claim 27 further comprising multiplying the first signal and a value from a look up table selected in accordance with the second signal to compensate for non-linearities in the signal path.